FLEX 10K & pci_a: The Complete PCI Solution

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The high-density and continuous routing structure of FLEX® 10K devices provide an ideal solution for peripheral component interconnect (PCI) designs. In fact, with the Altera `pci_a` MegaCore™ function, designers can quickly implement an entire PCI design on a single FLEX 10K device for maximum performance and design flexibility. In addition, the Altera OpenCore™ feature offers designers the security of "test-driving" the function before licensing it. This technical brief discusses the `pci_a` function and the EPF10K30 device in -3 speed grades as a complete PCI solution.

When considering PCI solutions, it is important to look at time-to-market aspects of the development process, e.g., ease-of-use, risk-free test drive, PCI performance, device availability, and hardware simulation and verification. Some PCI solutions appear to meet design-feature requirements, but are very time-consuming to implement and may not meet the 33-MHz PCI performance requirement. As an example, Altera Applications recently compared the Altera and Xilinx PCI solutions.

Ease-of-Use

The `pci_a` function is a "shrink-wrap" solution with real-time parameterization capability. Thus, designers can drop the `pci_a` function into a design file and define parameter values in real-time within the MAX+PLUS II development environment. In addition, because the `pci_a` function integrates a complete DMA controller, designers can connect the simple back-end interface to the custom portion of the design—providing a fully-operational PCI design in a short time frame. Even when implementing complex burst transfer designs, the `pci_a` function can be dropped into the design. On the other hand, when using the Xilinx PCI master/target megafunction to implement 33-MHz master/target designs—with or without burst transfer support—manual floorplanning is required. In addition, to customize the Xilinx PCI master/target megafunction, designers must specify parameter values via the world-wide web and then download the file with each modification.

Risk-Free Test Drive

Designers have the opportunity to instantiate and simulate the `pci_a` function before licensing it via the Altera OpenCore evaluation feature, available with every MAX+PLUS II design site. (Programming files as well as output files for third-party EDA tool simulation can only be generated with an authorization code, available with licensed functions.) In contrast, Xilinx does not offer a risk-free test drive of its PCI master/target function, i.e., designers must license the function before obtaining the file.

PCI Performance

The -3 speed grade EPF10K30 device meets the required maximum setup (7 ns) and minimum clock-to-output times (11 ns) as well as output drive characteristics. In addition, a design implemented with the `pci_a` function in the -3 speed grade EPF10K30 device meets the PCI bus performance requirement of 33 MHz.

Device Availability

The -3 speed grade EPF10K30 device, which is fully-compliant with the PCI Special Interest Group's (SIG) ***PCI Local Bus Specification, Revision 2.1*** for 33-MHz operation, is immediately available in volume quantities.

Hardware Simulation & Verification

The `pci_a` function is shipped with test vectors, a Windows-based software driver, and a prototyping board, which includes an EPF10K30RC240-3 device for PCI design simulation and verification. Altera is the only programmable logic device (PLD) vendor that includes a prototyping board with every licensed PCI function.

Table 1 summarizes the differences between the Altera and Xilinx PCI solutions.

Table 1. Altera & Xilinx PCI Solution Comparison

Features/Limitations/Pricing	Altera	Xilinx
Floorplanning	Not needed; function can be dropped-into the design	Required for fully-compliant, 33-MHz master/target designs, *Note (1)*
Hardware Verification Support	Yes, via the prototype board	No, *Note (2)*
User I/O Per Device Package	189	160
Device Volume Pricing	EPF10K30RC240-3 in 100+ units at $112	XC4013E-1PQ208 in 100+ units at $270, *Note (2)*
Function List Price	$7,995	$8,995, *Note (2)*

Notes:
(1) Source: Page 25 of the Xilinx *LogiCore PCI Master and Slave Interface User's Guide, version 1.1*
(2) Source: Xilinx world-wide web site, July 1997.

The documents listed below provide more detailed information. The part numbers are in parentheses.

- *PCI Master/Target MegaCore Function with DMA Data Sheet (A-DS-PCI1-01)*
- *Application Note 86: (Implementing the pci_a Master/Target in FLEX 10K Devices) (A-AN-086-01)*
- *Solution Brief 20: PCI Bus Master/Target MegaCore Function (A-SB-020-01)*
- *Technical Brief 25: Using the OpenCore Evaluation Feature (M-TB-025-01)*

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